

REMARKS

Applicant thanks the Examiner for examination of the
5 application.

Claims 2, 5, 13, 17 and 21-25 have been canceled.

The Examiner is requested to withdraw the rejection of
10 independent claims 16-18, 20-23, and 25 under 35 U.S.C. § 102(b)
as anticipated by Dent et al, U. S. Patent No. 5,187,675.

Amended Claim 16 recites:

15 In an array of N data values, a method of determining an
address for a result, the result being the output of a
binary operation defined in the array of data values each
data value having W bits, the method comprising the steps
of:

20 (a) performing, at each computation stage i of $\log_2 N$,
computation stages, $N/2^i$ binary operations on the data
values of $N/2^i$ pairs of input values using a binary
operator, wherein each input value includes a data value and
a partial address, wherein each of the binary operations
25 generates a binary decision representative of a selected
data value and the partial address of the selected data
value;

(b) multiplexing at each computation stage each pair of
input values using a multiplexer and producing an output
determined by the binary decision; and

30 (c) storing at each computation stage the binary
decision and the selected input in a storage element.

Dent et al. teaches a binary tree structure that is
symmetric, or regular when $M=2^N$ for determining the greatest or
35 the least. As shown in Figure 1, pairs of the M input values V_0 -
 V_7 are compared in a first stage of a tree 10 having $M/2=4$
comparators 11-1 to 11-4; the larger value of each pair is
selected and passed to a second stage having $M/4=2$ comparators
12-1, 12-2. The larger values of the two pairs are passed to the

final, third stage having $M/8=1$ comparator 13, which passes the largest values V_{MAX} to its output. It will be appreciated that the number of stages needed for searching the M input values is just N .

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Amended claim 16 requires a binary operator, a multiplexer and a storage element.

Dent et al. does not teach nor suggest a multiplexer nor a storage element as recited in amended Claim 16.

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Amended Claim 16 requires the step of "performing, at each computation stage i of $\log_2 N$, computation stages, $N/2^i$ binary operations on the data values of $N/2^i$ pairs of input values using a binary operator, wherein each input value includes a data value and a partial address, wherein each of the binary operations generates a binary decision representative of a selected data value and the partial address of the selected data value."

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Dent et al. does not teach an input value that includes a data value and a partial address.

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Furthermore, amended Claim 16 requires the step of "multiplexing at each computation stage each pair of input values using a multiplexer and producing an output determined by the binary decision."

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Dent et al. does not teach nor suggest a multiplexer nor the multiplexing step as required by Claim 16.

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Moreover, amended Claim 16 requires the step of storing at each computation stage the binary decision and the selected input in a storage element.

Dent et al. does not teach nor suggest the storing step nor the storage element.

5 Since the Dent patent does not show nor suggest the claimed features of amended Claim 16, Claim 16 is unanticipated and unobvious over Dent et al. as recited by Examiner.

10 Dependent claims 18 and 20 are also allowable as depending on allowable independent amended Claim 16 and including further limitations that distinguish over the art. Claim 18 provides that the computation stage at level $\log_2 N$ contains the value of the result of the binary operation and its address within the array of values. Claim 20 at least provides claim
15 differentiation.

The Examiner is requested to withdraw the rejection of claims 1-15 under 35 U.S.C. § 103(a) as being unpatentable over Dent et al. (U. S. Patent No. 5,187,675) in view of Weigand et
20 al. patent] (U. S. Patent No. 5,285,185).

Amended Claim 1 recites:

25 A system for locating a specific value contained in an array of N data values, the specific value being the result of a binary operation defined over the array of N data values wherein each data value is W bits wide, the system comprising a plurality of decision units grouped in successive computation stages wherein:

30 (a) each decision unit receives a pair of input values, each input value containing a data value and a partial address, wherein each of the plurality of decision units comprises:

35 (i) a binary operator for generating a binary decision representative of a local address of the selected data value,

(ii) a multiplexer coupled to the binary operator for generating one of the pair of input values as output and with the output being selected by the binary decision, and

(iii) a storage element coupled to the binary operator and the multiplexer for storing the output of the multiplexer and the binary decision which is added to the partial address of the selected data value; and

5 (b) each decision unit generates a value representative of a selected data value and the partial address of the selected data value and the decision unit of the last computation stage contains the specific value.

10 Dent et al. teaches a binary tree structure that is symmetric, or regular when $M=2^N$ for determining the greatest or the least. Dent et al. does not teach nor suggest the binary operator, the multiplexer nor the storage element as is required by the amended Claim 1. Clearly, the Dent patent does not teach
15 the configuration as required by amended Claim 1.

Weigand et al. teaches comparator for comparing dual-coded data, such as can be used for fast address comparison in computer systems, for testing and diagnosis of software, or in digital
20 control circuits for comparison of reference and actual values. Specifically, col. 2, lines 43-54, disclose the use of a partial address assigned to the partial comparison data. Weigand et al. does not teach nor suggest the configuration of the binary operator, the multiplexer, and the storage element as is required
25 by the amended Claim 1.

The combination of Dent et al. and Weigand et al. does not provide an apparatus with the required features of a system for locating a specific value contained in an array of N data values
30 required by amended Claim 1. The combination of Dent et al. and Weigand et al. does not teach nor suggest a "multiplexer coupled to the binary operator for generating one of the pair of input values as output and with the output being selected by the binary decision" as required by amended Claim 1. Furthermore, the
35 combination of Dent et al. and Weigand et al. does not teach nor suggest "a storage element coupled to the binary operator and the

multiplexer for storing the output of the multiplexer and the binary decision which is added to the partial address of the selected data value" as required by amended Claim 1. Accordingly, it would be necessary to make modifications not
5 taught in the prior art to combine the references in the manner suggested by the Examiner. Thus, it would not have been obvious to one skilled in the art to combine the references in the manner suggested.

10 Moreover, since the combination of Dent et al. and Weigand et al. does not show nor suggest the apparatus of amended Claim 1, Claim 1 is unanticipated and unobvious over Dent et al. in view of Weigand et al. as recited by Examiner.

15 Dependent claims 3, 4, and 6 - 11 are also allowable as depending on allowable independent amended Claim 1 and including further limitations that distinguish over the art. Claim 3 provides that the binary operator selects the minimum value of the pair of data values contained in the pair of input values.
20 Claim 4 provides that the binary operator selects the maximum value of the pair of data values contained in the pair of input values. Claim 6 provides that the partial address of an input value at computation stage i is the $(i-1)$ most significant bit of the storage element of computation stage $(i-1)$. Claim 7 provides
25 that the partial address of an input value at computation stage i is the $(i-1)$ least significant bit of the storage element of computation stage $(i-1)$. Claims 8 and 9 at least provide claim differentiation. Claim 10 provides that the last computation stage contains the address of the specific value in the K most
30 significant bits of its associated storage element. Claim 11 provides that the last computation stage contains the address of the specific value in the K least significant bits of its associated storage element.

Amended claim 12 recites:

5 An apparatus for obtaining information on a specific value within a pair of inputs, wherein each input contains a data value and a partial address of the data value, the apparatus comprising:

10 (a) a binary operator which compares the data values and which generates as output a binary decision representative of a local address of the specific data value;

15 (b) a multiplexer coupled to the binary operator and coupled to receive each data values along with its partial address which generates as output the specific data value along with its partial address based on the binary decision; and

(c) a storage element coupled to the binary operator and the multiplexer which stores the output of the multiplexer and the binary decision.

20 Dent et al. teaches a binary tree structure that is symmetric, or regular when $M=2^N$ for determining the greatest or the least. Dent et al. does not teach nor suggest the binary operator, the multiplexer nor the storage element as is required by the amended Claim 12. Clearly, the Dent patent does not teach
25 the configuration as required by amended Claim 12.

30 Weigand et al. teaches comparator for comparing dual-coded data, such as can be used for fast address comparison in computer systems, for testing and diagnosis of software, or in digital control circuits for comparison of reference and actual values. Specifically, col. 2, lines 43-54, disclose the use of a partial address assigned to the partial comparison data. Weigand et al. does not teach nor suggest the configuration of the binary operator, the multiplexer, and the storage element as is required
35 by the amended Claim 12.

The combination of Dent et al. and Weigand et al. does not provide an apparatus for obtaining information on a specific value within a pair of inputs required by amended Claim 12. The

combination of Dent et al. and Weigand et al. does not teach nor suggest a "multiplexer coupled to the binary operator and coupled to receive each data values along with its partial address which generates as output the specific data value along with its partial address based on the binary decision" as required by amended Claim 12. Furthermore, the combination of Dent et al. and Weigand et al. does not teach nor suggest "a storage element coupled to the binary operator and the multiplexer which stores the output of the multiplexer and the binary decision" as required by amended Claim 12. Accordingly, it would be necessary to make modifications not taught in the prior art to combine the references in the manner suggested by the Examiner. Thus, it would not have been obvious to one skilled in the art to combine the references in the manner suggested.

Moreover, since the combination of Dent et al. and Weigand et al. does not show nor suggest the apparatus of amended Claim 12, Claim 12 is unanticipated and unobvious over Dent et al. in view of Weigand et al. as recited by Examiner.

Dependent claims 14 and 15 are also allowable as depending on allowable independent amended Claim 12 and including further limitations that distinguish over the art. Claims 14 and 15 at least provide claim differentiation.

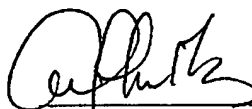
Applicants have carefully reviewed the additional references, Patent numbers 4,821,290, 5,455,825, 4,100,532, and 5,710,562 made of record by the Examiner and not relied upon for rejecting the claims. Applicants believe that neither of these references made of record, taken singly or in any permissible combination, affect the assertion of patentability of claims 1, 3-4, 6-12, 14-16 and 18-20 in the present application.

Claims 1, 3-4, 6-12, 14-16 and 18-20 stand allowable.

This Amendment, submitted in response to the outstanding
office action dated October 24, 2002 is believed fully responsive
5 to each point of objection or rejection raised therein.

The Claims 1, 3-4, 6-12, 14-16 and 18-20 distinguish over
the cited references and the application is in allowable form.
Applicant respectfully requests reconsideration or further
10 examination and allowance of the application.

Respectfully submitted,



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VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the Claims:

5 Claims 2, 5, 13, 17 and 21-25 have been canceled.

 Claims 1, 3, 4, 6, 7, 12, and 16 have been amended as follows:

1 1. (Amended) A system for locating a specific value contained in
2 an array of N data values, the specific value being the result of
3 a binary operation defined over the array of N data values
4 wherein each data value is W bits wide, the system comprising a
5 plurality of decision units grouped in successive computation
6 stages wherein:

7 (a) each decision unit receives a pair of input values, each
8 input value containing a data value and a partial address,
9 wherein each of the plurality of decision units comprises:

10 (i) a binary operator for generating a binary decision
11 representative of a local address of the selected data value,

12 (ii) a multiplexer coupled to the binary operator for
13 generating one of the pair of input values as output and with the
14 output being selected by the binary decision, and

15 (iii) a storage element coupled to the binary operator
16 and the multiplexer for storing the output of the multiplexer and
17 the binary decision which is added to the partial address of the
18 selected data value; and

19 (b) each decision unit generates a value representative of a
20 selected data value and the partial address of the selected data
21 value and the decision unit of the last computation stage
22 contains the specific value.

1 3. (Amended) The system of claim [2] 1, wherein the binary
2 operator selects that minimum value of the pair of data values
3 contained in the pair of input values.

1 4. (Amended) The system of claim [2] 1, wherein the binary
2 operator selects the maximum value of the pair of data values
3 contained in the pair of input values.

1 6. (Amended) The system of claim [5] 1, wherein the partial
2 address of an input value at computation stage i is the $(i-1)$
3 most significant bit of the storage element of computation stage
4 $(i-1)$.

1 7. (Amended) The system of claim [5] 1, wherein the partial
2 address of an input value at computation stage i is the $(i-1)$
3 least significant bit of the storage element of computation stage
4 $(i-1)$.

1 12. (Amended) An apparatus for obtaining information on a specific
2 value within a pair of inputs, wherein each input contains a data
3 value and a partial address of the data value, the apparatus
4 comprising:

5 (a) a binary operator which compares the data values and
6 which generates as output a binary decision representative of a
7 local address of the specific data value; [and]

8 (b) a multiplexer coupled to the binary operator and coupled
9 to receive each data values along with its partial address which
10 generates as output the specific data value along with its
11 partial address based on the binary decision; and

12 (c) a storage element coupled to the binary operator and the
13 multiplexer which stores the output of the multiplexer and the
14 binary decision.

1 16. (Amended) In an array of N data values, a method of
2 determining an address for a result, the result being the output
3 of a binary operation defined in the array of data values each
4 data value having W bits, the method comprising the steps of:

5 (a) performing, at each computation stage i of $\log_2 N$,
6 computation stages, $N/2^i$ binary operations on the data values of
7 $N/2^i$ pairs of input values using a binary operator, wherein each
8 input value includes a data value and a partial address, wherein
9 each of the binary operations generates a binary decision
10 representative of a selected data value and the partial address
11 of the selected data value [local address of a selected data
12 value within the pair of input values]; [and]

13 (b) multiplexing at each computation stage each pair of
14 input values using a multiplexer and producing an output
15 determined by the binary decision; and

16 (c) storing at each computation stage the binary decision
17 and the selected input in a storage element.